IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants: Thomas W. Williams et al.

Assignee: Synopsys, Inc.

Title: INTELLIGENT TEST VECTOR FORMATTING TO REDUCE TEST VECTOR SIZE AND ALLOW ENCRYPTION THEREOF FOR INTEGRATED CIRCUIT TESTING

Serial No.: 09/728,022 File Date: November 30, 2000

Examiner: John J. Tabone Jr. Art Unit: 2138

Docket No.: SYN-0174

Date: May 11, 2006

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NON-COMPLIANT APPEAL BRIEF

Sir:

This Response To Non-Compliant Appeal Brief is in response to the Notification of Non-Compliant Appeal Brief dated April 27, 2006.

The Notification of Non-Compliant Appeal Brief states that the Appeal Brief does not contain a concise explanation of the subject matter defined in each of the independent claims involved in the appeal. The Examiner also requested that references to the Specification include page and line numbers rather than the paragraph numbers provided in the published patent application. Under these conditions, as indicated in the MPEP 1205.03(B), a paper providing a summary of the claimed subject matter as required by 37 CFR 41.37(c)(1)(v) will

suffice. Therefore, Appellants provide below an amended Section V. Summary of the Claimed Subject Matter.

V. AMENDED SUMMARY OF CLAIMED SUBJECT MATTER

As taught by Appellants in the Specification, page 6, line 2 to page 7, line 11:

> [T]he present invention provides a testing solution that reduces the overall cost of testing which includes costs associated with the tester and costs associated with the test circuitry on silicon. With the ability to implement millions of gates on a chip, the incremental cost of Design for Test (DFT) is relatively small. The present invention leverages the relatively inexpensive silicon to reduce the cost of the testers by moving some of the tester functionality onto the DUT itself but, unlike BIST, maintain use of deterministic test data. The present invention advantageously reduces the memory required to store fully specified test patterns.
>
> A method and circuit are described herein for testing an integrated circuit device using intelligent test vector formatting that reduces the memory required to store test patterns and also provides an encryption vehicle for the test patterns. The novel circuit includes a first memory that stores a test vector mask. The test vector mask is a sequence of bits that indicates if corresponding test vector data is deterministic or random. The test vector data used by the present invention contains a portion that is deterministically generated by automatic test pattern generation (ATPG) software and a portion that is random. A first data value of the mask indicates deterministic data and a second data value of the mask indicates random data. A second memory contains a sequence of bits that represent the deterministic test vector data. The first and second memory could be separate locations of the same memory device. Alternative variations of this method prefix the positions of deterministic data and random data such that the mask information is minimized to represent the encoded positions.

> A random number generator (e.g., linear feed-back shift register, LFSR) is also provided that generates a reproducible sequence of pseudo random bits that is based on a seed value. With respect to encryption, the seed value can be viewed as a key that is required for proper generation of the test vectors. A selector circuit, e.g., a multiplexer, is used to select bits either from the second memory or from the random number generator. The selection is based on the value of a corresponding bit of the mask vector which is coupled to the select input of the selector. The output of the selector provides a fully specified test vector for application to the integrated circuit device under test (DUT). In one embodiment, … the random number generator can be fabricated on the DUT.

Referring to FIG. 3 (shown below for convenience) and as taught by Appellants in the Specification, page 20, lines 4-13:

> The system of FIG. 3 acts to reduce the throughput of the data flowing from the tester 14' to the DUT 16'. The embodiment of FIG. 3 reduces the tester throughput to the DUT 16' by incorporating the LFSR circuit 230 on the DUT 16' itself. A configurability mechanism for sending data from the tester 14' or the compressed data source on the DUT 16' can be built-in. The control of the source of test data to the design would lie in the hands of the control logic 250 of the tester 14'. The embodiment of FIG. 3 also offers an increase in performance. Specifically, this configuration allows for the possibility of obtaining and applying the data portion that is generated on the DUT 16' at a faster rate than that could be achieved from a low cost tester.

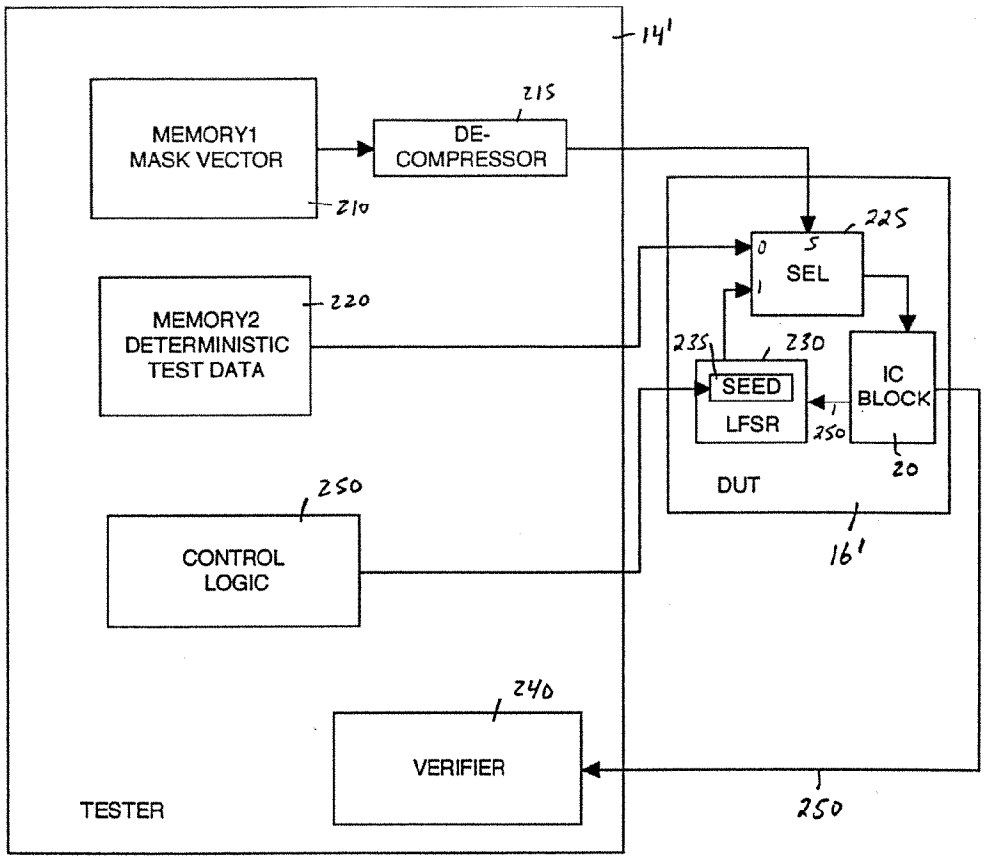


FIG. 3

Referring to FIG. 4B (shown below for convenience) and as taught by Appellants in the Specification, page 22, lines 4-16:

> FIG. 4B illustrates another embodiment of the LFSR circuit 230b which can interleave output values from the DUT 16 using OR gates 320-322. By interleaving the output values (e.g., over output lines 330-332) into the LFSR 230b, the effective "randomness" of the result is increased. This also increases error detection because an error on the output lines 330-332 will generate an improper input test pattern which will likely

lead to another departure from the expected result on the output, etc. This increases the likelihood that the error is detected by the verification circuitry 240 (FIG. 2, FIG. 3). The output lines 330-332 originate from the output of the DUT 16. The value of line 330 is ORed into the output of the first stage 310. The value of line 331 is ORed into the output of the second stage 311. The value of line 332 is ORed into the output of the third stage 312. It is appreciated that any number of stages can be used in accordance with this embodiment of the present invention.

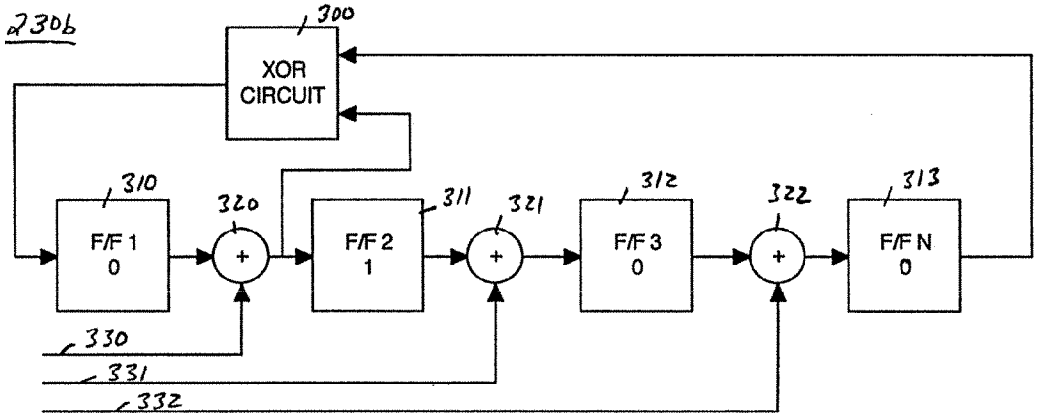


FIG. 4B

A concise explanation of the subject matter defined in each of Claims 7 and 17, referring to the Specification by page and line number and to the drawings, if applicable, follows below.

Claim 7: An integrated circuit testing system comprising: (see e.g. Specification, page 20, line 4 to page 21, line 5)

an integrated circuit tester (see e.g. FIG. 3, tester 14') comprising:

a first memory for storing therein a mask vector for characterizing corresponding test vector data (see e.g. FIG. 3, memory1 (mask vector) 210), said mask vector comprising a

plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random (see e.g. Specification, page 15, lines 17-23);

a second memory for storing therein deterministic test vector data (see e.g. FIG. 3, memory2 (deterministic test data) 220), said first and second memory coupled to a port (see e.g. Specification, page 16, lines 17-18 and page 17, lines 8-9);

an integrated circuit device under test (DUT) (see e.g. DUT 16') comprising:

a circuit block to be tested (see e.g. FIG. 3, IC block 20);

a random number generator for generating a reproducible sequence of pseudo random bits based on a seed number (see e.g. FIG. 3, LFSR 230 and seed 235); and

a selector circuit coupled to said port and for generating a test vector for application to said circuit block (see e.g. FIG. 3, selector circuit 225), said selector circuit for selecting bits as between said random number generator and said second memory based on said mask vector, said selector circuit having an output coupled to said circuit block.

Claim 17: A method for testing an integrated circuit comprising the steps of: (see e.g. Specification, page 20, line 4 to page 21, line 5 and page 22, lines 4-16)

retrieving a mask vector from a first memory (see e.g. FIG. 3, memory1 (mask vector) 210), said mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said

corresponding test vector data is pseudo random (see e.g. Specification, page 15, lines 17-23);

retrieving deterministic test vector data from a second memory (see e.g. FIG. 3, memory2 (deterministic test data) 220);

initializing a random number generator with a seed number and thereafter generating a reproducible sequence of pseudo random bits based on said seed number (see e.g. FIG. 3, LFSR 230 and seed 235);

generating an output test vector for application to a circuit block of said integrated circuit, said step d) comprising the step of selecting bits as between said random number generator and said second memory based on said mask vector (see e.g. FIG. 3, selector circuit 225 and IC block 20);

applying said output test vector to said circuit block (see e.g. FIG. 3, IC block 20, memory2 (deterministic test data) 220, LFSR 230);

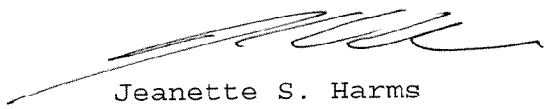
obtaining an output generated by said circuit block in response to said output test vector (see e.g. FIG. 3, output 250); and

supplying said output generated by said circuit block to an input of a stage of said random number generator (see e.g. FIG. 3, output 250, LFSR 230 and FIG. 4B, outputs 330, 331, 332, LFSR 230b).

CONCLUSION

Should the Examiner or Board desire additional clarification on the support for the claims, please contact the undersigned at 408-451-5907 (telephone).

Respectfully submitted,



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